

CLAIMS

1. A method comprising:

storing a rise time generic variable and a fall time generic variable, the rise
time generic variable comprising at least one rise time delay value and the fall time
generic variable comprising at least one fall time delay value;

selecting a rise time delay value and a fall time delay value in a VHDL
standard delay file that correspond to an instance of a logic gate in a logic model;

building a rise-time super generic value and a fall-time super generic value for
the selected rise time delay value and fall time delay value, the rise-time super
generic value representing a rise time delay value stored in the rise time generic
variable and the fall-time super generic value representing a fall time delay value
stored in the fall time generic variable.

2. The method of claim 1, further comprising:

storing the rise-time super generic value and fall-time super generic value in a
VHDL standard delay file to represent a rise time delay value and a fall time delay
value that correspond to the instance of a logic gate in a logic model.

3. The method of claim 2, wherein the rise-time super generic value comprises a
pointer to a rise time delay value stored in the rise time generic variable and the fall-
time super generic value comprises a pointer to a fall time delay value stored in the
fall time generic variable.

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4. The method of claim 1, further comprising:

repeating the selecting and building steps of claim 1 for every rise time delay value and fall time delay value in the VHDL standard delay file that correspond to every instance of every logic gate in the logic model.

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5. The method of claim 4, further comprising the step of:

storing every built rise-time super generic value and fall-time super generic value.

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6. The method of claim 5, wherein the storing step comprises the step of:

storing every built rise-time super generic value and fall-time super generic value in a VHDL standard delay file.

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7. The method of claim 5, wherein the collective stored every built rise-time super generic value and fall-time super generic value is a reduced storage size than the collective every rise time delay value and fall time delay value from the VHDL standard delay file.

8. A method comprising:

extracting correlation delays from a VHDL standard delay file analysis file;
generating a VHDL associative array structure; and
outputting a correlation VHDL file.

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9. The method of claim 8, wherein the VHDL associative array structure is a three dimensional data structure comprising:

a z-axis of the data structure representing a set of common blocks for each logical topology of a VHDL logic gate;

10 an x-axis of the data structure representing a delay name for the gate topology; and

a y-axis of the data structure representing an actual delay value.

10. The method of claim 8, wherein the correlation VHDL file comprises a VHDL package file embedded with correlation delay data.

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11. An apparatus comprising:

a controller/processor;

a data memory for storing a VHDL standard delay file and a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value;

a program memory storing an SDF reducer, the program memory communicatively coupled to controller/processor and the data memory, for selecting a rise time delay value and a fall time delay value in a VHDL standard delay file that correspond to an instance of a logic gate in a logic model, and for building a rise-time super generic value and a fall-time super generic value for the selected rise time delay value and fall time delay value, the rise-time super generic value representing a rise time delay value stored in the rise time generic variable and the fall-time super generic value representing a fall time delay value stored in the fall time generic variable.

12. The apparatus of claim 11, wherein the SDF reducer stored in the program memory for storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file in the data memory to represent a rise time delay value and a fall time delay value that correspond to the instance of a logic gate in a logic model.

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13. The apparatus of claim 12, wherein the rise-time super generic value comprises a pointer to a rise time delay value stored in the rise time generic variable and the fall-time super generic value comprises a pointer to a fall time delay value stored in the fall time generic variable.

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14. The apparatus of claim 11, wherein the SDF reducer, stored in the program memory, for storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file in the data memory to represent all rise time delay values and fall time delay values that correspond to each instance of every logic gate in a logic model.

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15. The apparatus of claim 14, wherein the reduced standard delay file comprises at most, two generics per logic gate instance.

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16. The apparatus of claim 11, further comprising:

a VHDL correlation generator, stored in the program memory, for extracting correlation delays from the VHDL standard delay file analysis file, generating a VHDL associative array structure, and outputting a correlation VHDL file; and

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a VHDL correlation file, communicatively coupled to the VHDL correlation generator.

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17. The apparatus of claim 16, wherein the VHDL correlation file comprises a VHDL package file embedded with correlation delay data.

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18. A system comprising:

a data memory for storing a VHDL standard delay file;

a VHDL standard delay file analysis file;

a program memory storing an SDF reducer, the program memory
communicatively coupled to the VHDL standard delay file and the VHDL standard
delay file analysis file, for selecting a rise time delay value and a fall time delay value
in a VHDL standard delay file that correspond to an instance of a logic gate in a logic
model, and for building a rise-time super generic value and a fall-time super generic
value for the selected rise time delay value and fall time delay value, the rise-time
super generic value representing a rise time delay value stored in the rise time
generic variable and the fall-time super generic value representing a fall time delay
value stored in the fall time generic variable; and

a reduced standard delay file, communicatively coupled to the SDF reducer.

19. The system of claim 18, wherein the SDF reducer stored in the program
memory for storing the rise-time super generic value and fall-time super generic
value in a VHDL standard delay file in the data memory to represent a rise time
delay value and a fall time delay value that correspond to the instance of a logic gate
in a logic model.

20. The system of claim 19, wherein the rise-time super generic value comprises a pointer to a rise time delay value stored in the rise time generic variable and the fall-time super generic value comprises a pointer to a fall time delay value stored in the fall time generic variable.

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21. The system of claim 18, wherein the SDF reducer, stored in the program memory, for storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file in the data memory to represent all rise time delay values and fall time delay values that correspond to each instance of every logic gate in a logic model.

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22. The system of claim 21, wherein the reduced standard delay file comprises at most, two generics per logic gate instance.

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23. The system of claim 18, further comprising:

a VHDL correlation generator, stored in the program memory, for extracting correlation delays from the VHDL standard delay file analysis file, generating a VHDL associative array structure, and outputting a correlation VHDL file; and

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a VHDL correlation file, communicatively coupled to the VHDL correlation generator.

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24. The system of claim 23, wherein the VHDL correlation file comprises a VHDL package file embedded with correlation delay data.

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25. A computer readable medium comprising instructions for:

storing a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value;

5 selecting a rise time delay value and a fall time delay value in a VHDL standard delay file that correspond to an instance of a logic gate in a logic model;

building a rise-time super generic value and a fall-time super generic value for the selected rise time delay value and fall time delay value, the rise-time super generic value representing a rise time delay value stored in the rise time generic variable and the fall-time super generic value representing a fall time delay value stored in the fall time generic variable.

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26. The computer readable medium of claim 25, further comprising instructions for:

15 storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file to represent a rise time delay value and a fall time delay value that correspond to the instance of a logic gate in a logic model.

27. The computer readable medium of claim 26, wherein the rise-time super generic value comprises a pointer to a rise time delay value stored in the rise time generic variable and the fall-time super generic value comprises a pointer to a fall time delay value stored in the fall time generic variable.

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28. The computer readable medium of claim 25, further comprising instructions for:

repeating the selecting and building steps of claim 1 for every rise time delay value and fall time delay value in the VHDL standard delay file that correspond to every instance of every logic gate in the logic model.

29. The computer readable medium of claim 28, further comprising instructions for:

storing every built rise-time super generic value and fall-time super generic value.

30. The computer readable medium of claim 29, wherein the storing step comprises the step of:

storing every built rise-time super generic value and fall-time super generic value in a VHDL standard delay file.

31. The computer readable medium of claim 29, wherein the collective stored every built rise-time super generic value and fall-time super generic value is a reduced storage size than the collective every rise time delay value and fall time delay value from the VHDL standard delay file.

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32. A computer readable medium comprising instructions for:
extracting correlation delays from a VHDL standard delay file analysis file;
generating a VHDL associative array structure; and
outputting a correlation VHDL file.

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33. The computer readable medium of claim 32, wherein the VHDL associative array structure is a three dimensional data structure comprising:

a z-axis of the data structure representing a set of common blocks for each logical topology of a VHDL logic gate;

an x-axis of the data structure representing a delay name for the gate topology; and

a y-axis of the data structure representing an actual delay value.

34. The method of claim 32, wherein the correlation VHDL file comprises a VHDL package file embedded with correlation delay data.